REMARKS

In response to the Office Action mailed on 21 September, 2005, Applicant wishes to enter the following remarks for the Examiner's consideration. Applicant has amended the abstract to be a single paragraph. Applicant has amended claims 1, 6 and 15, 18, 19 and 21. Claims 1-23 are pending in the application.

Rejection of claims under 35 USC §102(b)

Claims 1-5, 9-10, 15-17 and 21-22 have been rejected under 35 USC §102(b) as being anticipated by Watkins, US Patent No. US 5,937,436. Applicant respectfully traverses this rejection of the claims in view of the amendments to claims 1 and 15.

Claim 1 has been amended to clarify that the address translation unit is coupled between the first and second interfaces. This change is supported by Figure 2 of the specification and the associated description thereof (for example, page 4, line 19 to page 5, line 7). In Figure 2, the address translation filter 118 is placed on the bus structure 108. The address translation filter of claim 1 is for filtering a signal on a system bus. In contrast, Watkins discloses devices for converting signals from one bus of protocol to a different bus or protocol. Watkins figure 2a shows a number of interfaces to the system bus 230 (e.g. CPU's 210_i, and the interfaces to the memory 230 and the bridge 240. However, the there are no elements connected between any of these interfaces. The bridge 240 has two interfaces and connects between the system bus 230 and the I/O bus 270. However in claim 1, as amended, the first and second interfaces are interfaces with the same system bus. The Network Interface Circuit 260_k in figures 2a and figure 4 is coupled

between an I/O bus 270 and at ATM interface 320. In contrast to the address translation filter of claim 1, the Network Interface Circuit only has one interface to the bus 270. Further, the I/O bus 270 does not couple between a core processor and an external memory unit, as is called for in claim 1.

Claims 5 depends from claim 1. Although additional arguments could be made for the patentability of claim 5, such arguments are believed unnecessary in view of the above discussion.

Claim 9 calls for the address translation unit to be operable to translate a virtual memory address received *via the system* bus from the external processing device into a physical memory address that is transmitted *via the system bus* to the external memory unit. Thus, the address translation unit acts as a filter on the system bus. The address translation unit receives a signal from the bus as input and provides a signal to the bus as output. This is in contrast to Figure 4 of Watkins, which shows an address translation unit 450 in an address generation unit 440. The address generation unit provides interface between the I/O bus 270 and an ATM core. Watkins does not teach a filter on the system bus.

Claim 10 depends from claim 9. Although additional arguments could be made for the patentability of claim 10, such arguments are believed unnecessary in view of the above discussion.

Claim 15 been amended to clarify the first bus signal is received from a bus and that the second bus signal is transmitted to the same bus. This is not taught by Watkins. Watkins teaches the use of an address translation unit to translate from a virtual address to physical address, but he does not teach that the address translation unit operates as a filter on a bus. Figure 4 of the

Watkins reference shows an address translation unit 450 in an address generation unit 440. The address generation unit provides an interface between the I/O bus 270 and an ATM core. It does not receive a bus signal from the bus, translating a virtual memory address specified by the bus signal to a physical memory address in an address translation filter, and then transmit a bus signal to the bus in accordance with the physical memory address, as called for by claim 15. Rather, the signals are received by the address generation unit 440 from the ATM core and then transmitted to the bus 270.

Claims 16-17 and 21-22 depend from claim 15. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. Claim 21 has been amended to provide correct antecedent basis in view of the amendment to claim 15.

In light of the foregoing amendment and remarks, Applicant respectfully submits that the Watkins reference does not teach, suggest, disclose or otherwise anticipate the recitations of claims 1-5, 9-10, 15-17 and 21-22. Applicant thus respectfully requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for these claims be mailed at the Examiner's earliest convenience.

Rejection of claims under 35 USC §103(a)

Claims 7, 14, 20 and 23 have been rejected under 35 USC §103(a) as being unpatentable over Watkins, US Patent No. U.S. 5,937,436. Applicant

respectfully traverses this rejection of the claims in view of the amendments to claims 1 and 15.

Claim 7 depends from claim 1. As discussed above, claim 1 has been amended to clarify that the address translation unit is coupled between the first and second interfaces. The address translation filter operates as a filter on a system bus. In contrast Watkins discloses a networking interface circuit NIC) that operates between an I/O bus and an ATM core (see figures 3 and 4 and the associated description thereof). The objective is to provide an interface between different protocols (the I/O bus protocol and the ATM protocol). The Watkins reference provides nothing to motivate one of ordinary skill in the art to consider a bus filter. A bus filter as claimed in claim 1 and dependent claim 7 receives a signal from the bus as input and provides a signal to the same bus as output. Thus, the input and output operate under the same protocol.

The applicant submits that it would not be obvious for one of ordinary skill in the art for the address translation filter to both receive and transmit a system clock signal, as called for in claim 7.

Claim 14 depends from independent claim 9 discussed above. As described above with reference to claim 7, the Watkins reference discloses an interface between dissimilar protocols, and does not teach, disclose or otherwise suggest the use of an address translation filter operating on a single bus.

Claims 20 and 23 depend from claim 15 discussed above. Claim 15 been amended to clarify the first bus signal is received from a bus and that the second bus signal is transmitted to the same bus. This distinguishes the

claim from the NIC disclosed by Watkins, since the Watkins reference discloses an interface between dissimilar protocols, and does not teach, disclose or otherwise suggest the use of a bus filter operating on a single bus. Claim 15 has been further amended to clarify that the bus couples between a core processor and the external memory unit. Referring to figure 2a of the Watkins reference, the NIC operates between the I/O bus 270 and an ATM core, while the bridge interfaces between dissimilar bus architectures (230 and 270).

Regarding claim 23, transferring an initial memory map to an internal device, such as 112 in Figures 1 and 2 of the application, is not equivalent to transferring an initial memory map to an external address translation filter 118.

Claims 6, 8, 11-13 and 18-19 have been rejected under 35 USC §103(a) as being unpatentable over Watkins, US Patent No. US 5,937,436 in view of McGrath, US Patent No. 6,671,791. Applicant respectfully traverses this rejection of the claims in view of the amendments to claims 1 and 15.

The Examiner acknowledges that the Watkins reference fails to teach, disclose or suggest the recitation of the claims, and relies upon the teachings of McGrath to overcome this defect. As discussed above with reference to independent claims 1, 9 and 15 from which claims 6, 8, 11-13 and 18-19 depend, Watkins does not teach, disclose or suggest the use of a filter on a bus. Instead, he teaches an interface to a bus and a bridge between dissimilar buses. In addition to this, the Examiner acknowledges that the Watkins reference fails to teach, disclose or suggest the use of an output control link, and relies upon the teachings of McGrath to overcome this defect.

Referring to figure 3 of the McGrath reference, the MMU 20 is integral to a processor 10 and communicates with an execution core 14 that is also integral to the processor 10. The function of the MMU 20 is similar to that of the virtual to physical memory map 112 shown in Figures 1 and 2 of the application. In particular, the MMU does not lie on the system bus between a core processor and an external memory unit, as is called for in claims 1 and 15. Further, the MMU 20 is not external to the processor 10. The MMU 20 is not accessible to external devices (such 114 and 116 in Figure 2 of the application) that are coupled to the bus structure. This forces these devices to address the external memory using physical addresses and complicates the programming of the devices.

McGrath teaches signaling between the execution core and an MMU that is integral to processor 10, but does not teach signaling between a core processor and an external address translation filter.

Claim 6 has been amended to provide correct antecedent basis in view of the amendment to claim 1.

Claims 18 and 19 has been amended to provide correct antecedent basis in view of the amendment to claim 15.

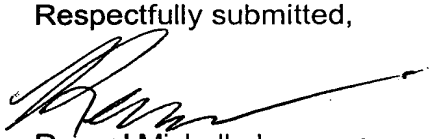
Applicant respectfully submits that the Watkins and McGrath references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim 6, 8, 11-13 and 18-19. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claim 6, 8, 11-13 and 18-19 be mailed at the Examiner's earliest convenience.

In light of the foregoing amendments and explanations, applicant submits that all rejections of claims 1-23 have been overcome. The scope of the amended claim 1, 6 and 15 is substantially the same with implicit meaning now made explicit. Allowance of claims 1-23 is therefore respectfully requested at the Examiner's earliest convenience. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action.

Applicant additionally submits formal drawings to replace the informal drawings originally filed with the application.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,



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